**For Quartus II versions 7.1 and 9.1**

1. Click on new project wizard under file menu then select next.
2. In the first menu box create a new directory and select open.
3. In the second menu box give the project a name, this will default with to the same name for the top-level design entry, then select next.
4. Enter a file name if one exists, otherwise select next.
5. Do not select any device or EDA tools.
6. When loaded select the file tab in the Project Navigator.
7. In the file menu select New->Verilog HDL file and then select OK. It will default to Verilog1.v but it can be saved under any name with a .v extension.
8. In the first line enter the top level name for the module – this should match the project name for convenience i.e. if the project name is demo1 then the module should be named demo1.
9. Enter your Verilog code, terminating each line with a semicolon and terminate the module use the reserved word endmodule without semicolon.
10. Select compile (the purple triangle) and wait till it finishes.
11. When finished select new file from file menu, other file, and select vector waveform file.
12. Save this to whatever name you wish – it will default to the project name.
13. From the top level menu select assignments and select settings and in the left hand panel select simulator settings and make sure the saved .vwf file name is entered in the simulation input box.
14. Select OK and you should now be back in the .vwf file.
15. In the name column select insert node or bus, select node finder and then select list.
16. Highlight all nodes and select the >> button to put them into the selected nodes panel. Select OK, and OK again.
17. Each node line should now appear in the .vwf file. Select each input node and set up the input sequence. Use right click to select the sequence. Value is a useful start.
18. Save this setup and now select the blue triangle on its side with the square waveform underneath. This will run the timing simulation.
19. Note the coverage – if this < 50% check you logic. To zoom in select control space, to zoom out select control shift space bar.
20. Under tools select the netlist view and a diagram of the hardware instantiated should now be drawn.